TRANSMIT VIRTUAL CONCATENATION PROCESSOR

ABSTRACT OF THE DISCLOSURE

[62] A transmit virtual concatenation processor for multiplexing channelized data onto a SONET/SDH frame is disclosed. The processor is scalable and is able to handle mapping a number of data channels to a number of different frame sizes including STS-12, STS-48, STS-192 and STS-768. The processor supports virtual concatenation with arbitrary channel mapping at both STS-1 and STS-3c granularities. The processor also supports contiguous concatenation with STS-12c, STS-24c, STS-48c, STS-192c, etc. capacities (i.e., STS-Nc where N is a multiple of 3). In addition, the processor supports mixed concatenation where some channels are using contiguous concatenation and some other channels are using STS-3c-Xv virtual concatenation. Alternatively, the processor is able to support any virtual concatenation, any contiguous concatenation and any mixed concatenation. The processor terminates the H1, H2 and H3 bytes in the line overhead of a SONET/SDH frame and inserts the multi-frame indicator and sequence number in the H4 byte of the path overhead.